American International University- Bangladesh (AIUB)
Faculty of Engineering (EEE)

Course Name:	Digital Logic Circuits	**Course Code:**	EEE 3101		
Semester:	Spring 24-25	**Assignment Name:**	OBE Assignment		
Marks:	30	**Term:**	Final		
Faculty:		**Section**			
Student Name:		**Student ID:**		**Serial :**	
Submission Date:		**Department:**			

COs/ CLOs Number	COs/CLOs Statements	K	P	A	Assessed Program Outcome Indicator	BNQF Indicator	Teaching-Learning Strategy
CO2	**Develop a digital system with conflicting requirements of a complex engineering problem.**	**3**	**P1,P2, P6**	**-**	**P.a.3.C3**	**FS.1**	**OBE Assignment** (Final Term)

Instructions Related to Use Variables:
Note that this problem uses the variables a, b, c, d, e, f, g and h, which are the digits of your student ID (ab-cdefg-h).
Any value in student ID comes '0' will be replaced by '(a+b+h)'

a	b	-	c	d	e	f	g	-	h

Marking Rubrics (to be filled by Faculty):

Complex Problem	Task	Assessment Criteria	Evaluation Criteria				Marks
P1, P2, P6	**I.**	Outline the necessary steps of the block diagram and flow diagram.	**Excellent (2.5)**	**Good (2-1.5)**	**Average (1-.5)**	**Poor (0)**	
			All the steps have been identified and are in the correct sequence	Not all the steps have been identified and in the correct sequence	Few steps have been identified and in the correct sequence	All the steps have been found in the wrong sequence.	
		Design counter with the necessary diagram	**Excellent (2.5)**	**Good (2-1.5)**	**Average (1-.5)**	**Poor (0)**	
			All the designs were accurate and working	Not all the designs were accurate and working	Few designs were accurate and working	All the designs were wrong and not working	
	II.	Design of System with timer circuit 1 & 2	**Excellent (12-10)**	**Good (9.5-6)**	**Average (5.5-3)**	**Poor (2.5-0)**	
			Circuit design is correct and complies with the problem	Circuit design is correct, but does not comply with the problem	Circuit design is incorrect and does not comply with the problem	Circuit design is wrong and does not comply with the problem	
	III.	FSM design and HDL Code	**Excellent (8-7)**	**Good (6.5-4)**	**Average (3.5-2)**	**Poor (1.5-0)**	
			Design is correct and complies with the requirements, with no or minor calculation errors.	Design is correct and complies with the requirements, but with major calculation errors.	Design has major flaws which does not comply with the requirements, but with minor calculation errors.	Design has major flaws which does not comply with the requirements, with major calculation errors.	
	IV.	Limitations of the developed system	**Excellent (5-4)**	**Good (3.5-2)**	**Average (1.5-1)**	**Poor (0)**	
			Provides limitations and analyzes the performance correctly	Provides limitation only	Provides improper limitations and performance analysis	Provides no limitation and gives no performance analysis	

Marks Obtained:

Digital Parking Control System:

Prepare a design to monitor available spaces in a parking garage that can house up to (**a+g+h**) cars. In the figure, the keypad is used to provide your maximum available space. When the garage is full of cars, it continuously displays the word "FULL" in a display sign with the seven-segment display. Otherwise, it will display "SPACE AVAILABLE" in a blinking fashion through another display sign with the seven-segment display. There are sensors in entry and exit points that can be used to count the number of cars getting in and out.

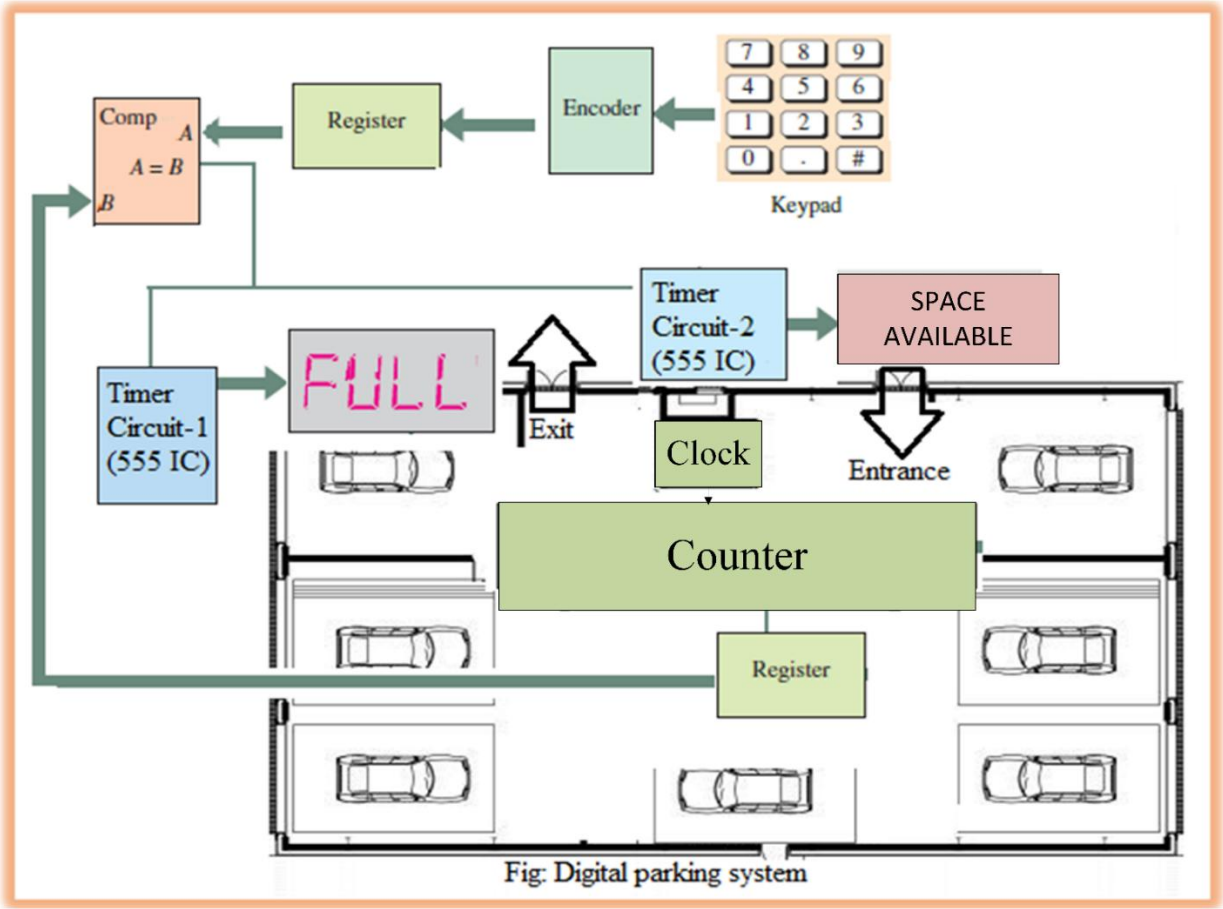

Fig: Digital parking system

Your task is to:

i. Outline the essential steps in the appropriate sequence to develop a block diagram and a flow diagram for designing an automated parking control system as described above. This system should activate the two seven-segment displays (displaying either "FULL" or "SPACE AVAILABLE") based on sensor data collected at the entry and exit points. Use a counter to collect the sensor data (how many cars are entering and exiting). Show the internal architecture of the counter (how flip-flops are connected to form the counter).

ii. Design a circuit to activate the two seven-segment displays using two 555 timers (one circuit to display FULL, another to display SPACE AVAILABLE). When the garage is full of cars, it should continuously display the word "FULL". If space is available for cars, it should display the word "SPACE AVAILABLE" in a blinking fashion. For the second timer (meant for displaying "SPACE AVAILABLE"), duty cycle D (%) = 100 – P, where P = (a+c+d+e+f) *2 and frequency f = a + d + 2 Hz. The display will be ON for T_H ms and OFF for T_L ms. Select a relevant resistor value to produce the output with the desired duty cycle. Select a capacitor value from 50 µF, 250 µF, and 470 µF. Include any additional sequential and combinational logic components, as needed, to ensure smooth control and operation, providing appropriate reasoning for selecting those components.

iii. Prepare an FSM design that outputs A for T_H ms and then B for T_L ms. Here, the clock period is 1 ms. Show the state diagram, state table, and Verilog HDL code only for the outputs (A, B). Note that if $T_H > 4$, Set $T_H = 4$. (For this Task only) If $T_L > 4$, Set $T_L = 4$. (For this Task only)

iv. Identify any drawbacks or limitations for the parts (i) and (ii). What modification can be made to the system to employ it in parking spaces with a higher number of cars than the current system? Analyze the impact of this specification change on the system.

Note the following.

- **The 555 timers do not have any control input that can continuously sustain an output value (it has no enable signal).**
- **D flip-flops can latch (store) data.**
    - **Simple D flip-flops transfer input values (D) to output (Q) at every active clock edge.**
    - **D flip-flops with enable signals (EN) transfer input values (D) to output (Q) at every active clock edge if EN is HIGH, otherwise the previous output is retained. If the reset (RST) signal is present, it will reset the output at an active clock-edge if EN is LOW.**